

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 03-248213

(43)Date of publication of application : 06.11.1991

(51)Int.Cl.

G06F 1/06
H03K 5/00

(21)Application number : 02-046781

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(22)Date of filing : 27.02.1990

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(54) TIMING SIGNAL GENERATING CIRCUIT

(57)Abstract:

PURPOSE: To obtain a small-sized inexpensive timing signal generating circuit which generates $2n$ -number of timing signals by taking in two sets of timing data, each consists of n -number of data written in a storage means, with two kinds of clock signal.

CONSTITUTION: A counting means 1 is operated with a $2f$ clock signal, and the LSB of the output is inputted to that of a storage means 2. n -number of data written in the address of the means 2 designated by the means 1 and n -number of data written in the other address are alternately outputted. An FF circuit 3 takes in former n -number of data with the LSB of the output of the means 1 as the clock signal. An FF circuit 5 takes in latter n -number of data with the signal, which is obtained by inverting the LSB of the output of the means 1 by an inverter 4, as the clock signal. An FF circuit 6 matches the phase of the output of the FF circuit 3 to that of the FF circuit 5 to output it. Thus, $2n$ -number of timing signals TIM1 to TIM $2n$ are generated.



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